REMARKS

Claims 1-13 and 22-28 are pending. The Office Action dated November 21, 2005, in this Application has been carefully considered. The above amendments and the following remarks are presented in a sincere attempt to place this Application in condition for allowance. In this response, claims 1-13 have been amended, claims 14-21 have been canceled, and claims 22-28 have been added. Reconsideration and allowance are respectfully requested in light of the above amendments and the following remarks.

In the Office Action, claims 8 and 12 were objected to due to informalities. In response thereto, Applicant notes that claims 8 and 12 have been amended herein. Applicant believes claims 8 and 12, as amended herein, are in condition for allowance.

In the Office Action, claim 13 was rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. Applicant notes that claim 13 has been amended herein. Applicant believes claim 13, as amended herein, is in condition for allowance.

In the Office Action, claims 1-21 were rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. The Examiner specifically rejected claims 1, 3-4, 9, 11, 12, 14, and 16 under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections.

In response thereto, Applicant notes that claims 1-13 have been amended herein, claims 14-21 have been canceled herein, and new claims 22-28 have been added herein. Applicant believes pending claims 1-13 and 22-28 are in condition for allowance.

As amended herein, independent claim 1 recites:

1. A processing system, comprising:

a processor comprising logic coupled to receive a clock signal via a plurality of local clock buffers, wherein the processor is configured to operate in a first power mode and a second power mode, and wherein the processor dissipates different amounts of electrical power in the first and second power modes;

a pulse train generator configured to produce three or more pulse trains, wherein each of the three or more pulse trains corresponds to a different level of electrical power dissipation within the processor;

selection logic coupled to receive each of the pulse trains produced by the pulse train generator and configured to produce a selected one of the pulse trains;

control logic coupled to the selection logic and configured to control the selection logic to effect transitions between the first and second power modes, wherein during each transition between the first and second power modes the selection logic produces at least three of the three or more pulse trains produced by the pulse train generator in sequence such that the electrical power dissipation of the processor changes monotonically during the transition; and

a timed clock control distribution network coupled to receive the sequence of pulse trains produced by the selection logic and configured to provide the sequence of pulse trains to the local clock buffers such that each of the local clock buffers receives the sequence of pulse trains at the same time.

Fig. 2 of the instant Application shows a system 200 including a processor 101 (i.e., a processing system). The processor 101 includes logic (see the specification, pg. 8, lines 2-4) coupled to receive a clock signal via multiple local clock buffers 290 (see the specification, pg. 12, lines 28-30). The processor 101 is configured to operate in multiple power states or modes

including a "full power" state or mode and a "nap" state or mode (see the specification, pg. 8, lines 8-10). The processor dissipates different amounts of electrical power in the full power and nap modes (see Figs. 4 and 5 and the corresponding specification text, pp. 15-16, lines 14-2).

The processing system of Fig. 2 also includes a pulse train generator 250. In the embodiment of Fig. 2, the pulse train generator 250 is configured to produce four pulse trains labeled "1," "2/3," "1/3," and "0" in Fig. 2. Each of the pulse trains corresponds to a different level of electrical power dissipation within the processor 101 (see Figs. 4 and 5, where each of the 4 pulse trains is sequentially applied to the local clock buffers 290). Applicant notes that at least three pulse trains may be sufficient to mitigate an otherwise abrupt transition between two different levels of electrical power dissipation within the processor 101.

The processing system of Fig. 2 also includes selection logic (i.e., the multiplexer 255) coupled to receive each of the pulse trains produced by the pulse train generator 250, and configured to produce a selected one of the pulse trains. The processing system of Fig. 2 also includes control logic (including the state machine ramp control 260 and the delay counter 240) that is coupled to the selection logic, and configured to control the selection logic to effect transitions between at least the full power mode and the nap mode. In the embodiment of Fig. 2, during each transition between the full power mode and the nap mode, the multiplexer 255 produces the four pulse trains produced by the pulse train generator 250 in sequence such that the electrical power dissipation of the processor 101 changes monotonically during the transition (see Figs. 4 and 5). Applicant again notes that at least three pulse trains produced in sequence may be sufficient to mitigate an otherwise abrupt transition between two different levels of electrical power dissipation within the processor 101.

The processing system of Fig. 2 also includes a timed clock control distribution network 270 coupled to receive the sequence of pulse trains produced by the multiplexer 255 and configured to

provide the sequence of pulse trains to the local clock buffers 290 such that each of the local clock buffers 290 receives the sequence of pulse trains at the same time. (See the specification, pg. 10, lines 5-11.)

In the present response, Applicant addresses all of the claim objections and rejections cited in the Office Action. In view of the amendments to the claims and Applicant's remarks, Applicant believes pending claims 1-13 and 22-28 are in condition for allowance, and respectfully request allowance of pending claims 1-13 and 22-28.

With the amendments to the claims presented herein, there are currently 3 pending independent claims and 20 total pending claims in the application. As the original application had 3 independent claims and 21 total claims, Applicant believes no additional fees are due. In the event that any other fees are due, the Commissioner is hereby authorized to charge any required fees due (other than issue fees), and to credit any overpayment made, in connection with the filing of this paper to Deposit Account No. 50-0605 of CARR LLP.

The present amendment is believed to contain a complete response to the issues raised in the Office Action. Full reconsideration is respectfully requested. If the Examiner should have any questions, comments or suggestions, the undersigned attorney earnestly requests a telephone conference. In particular, should the Examiner deem that any further amendment is desirable to place this application in condition for allowance, the Examiner is also invited to telephone the undersigned at the number listed below.

Respectfully submitted,

CARR LLP

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Amendments To The Drawings

No amendments have been made to the drawings.